15. (Amended) A TFT LCD having a first substrate, a second substrate, and liquid crystal sealed between the first and second substrates, comprising:

a scanning line on the first substrate;

A7

a gate insulating layer on the scanning line;

figs. 2A, 2B

a channel layer on the gate insulating layer;

a signal line formed to cross the scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern;

a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line;

a protection film formed on an entire surface of the first substrate inclusive of the drain electrode; and

a pixel electrode formed on the protection film connected to the drain electrode;

wherein the drain electrode is parallel to the signal line.

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Office Action of February 19, 2002 has been received and contents carefully reviewed.

Claims 2-7, and 9-20 are currently pending in this application. Claims 1 and 8 have been canceled. Claims 2-7, 9-13, and 15 have been amended. Reconsideration and reexamination of this application is respectfully requested.

The Examiner objected to the title of the invention as not being descriptive. Applicant respectfully disagrees with the Examiner. However, to further prosecution of this application,

the title has been changed.

The Examiner objected to the disclosure because of informalities on page 5, lines 17 and 23, and in Figure 2B. Applicant has amended the specification and the drawings to correct the informalities noted by the Examiner and other informalities in the translation. No new matter has been added.

The Examiner rejected claims 8-14 under 35 U.S.C. § 112, paragraph as being indefinite. In light of the cancellation of claim 8, the rejection is now moot. Applicant submits that all of the claims comply with 35 U.S.C. § 112.

The Examiner rejected claims 1, 2, 4-10, 12, and 13 under 35 U.S.C. § 102(e) as being clearly anticipated by Endo et al. (U.S. Patent No. 6,016,174). The Examiner rejected claims 3, 11, and 14-20 under 35 U.S.C. 103(a) as being unpatentable over Endo et al. (U.S. Patent No. 6,016,174). Applicant respectfully traverses these rejections.

Independent claims 2, 9, and 15 are allowable at least for the reason that claims 2, 9, and 15 recite a combination of elements including wherein the drain electrode is parallel to the signal line. None of the cited references teaches or suggests each and every element of the claims. None of the cited references, singly or in combination, teaches or suggests at least these features.

In Endo et al., the drain line (electrode) 215 is not parallel with the source line (signal line) 214. In contrast, the drain electrode 117b of claims 2, 9, and 15 of this application is parallel with the signal line 117a. Applicant submits that independent claims 2, 9, and 15 are allowable over the cited references.

Moreover, claims 3-7, 9-14, and 16-20 are allowable by virtue of their dependence on claims 2, 9, and 15, which are believed to be allowable.

Applicant respectfully requests that the rejections under 35 U.S.C. §§ 102(e) and 103(a) be withdrawn.

The dependent claims have been amended to change their dependency for consistency.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."** No new matter has been added.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 624-1232.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Dated: May 16, 2002

Respectfully submitted,

By _____
Teresa M. Arroyo
Registration No.: 50,015

LONG ALDRIDGE & NORMAN LLP
701 Pennsylvania Avenue N.W.
Suite 600, Sixth Floor
Washington, DC 20004
Telephone (202) 624-1200
Facsimile (202) 624-1298
Attorneys for Applicant

Version With Markings to Show Changes Made

In the Specification

Page 2, Paragraph beginning at line 3:

The present invention relates to a liquid crystal display, and more particularly, to a TFT (Thin Film Transistor) LCD (Liquid Crystal Display) having a large aperture ratio.

Page 2, Paragraph beginning at line 6:

Referring to FIG. 1A, an AMLCD (Active Matrix Liquid Crystal Display Device) used in a portable TV or a notebook computer, or the like is provided with a plurality of scanning lines 10 and signal lines 17 crossing each other, and pixel regions defined by the scanning lines 10 and the signal lines 17. These are TFTs at parts where the scanning lines 10 and the signal lines are crossed; and pixel electrodes (dashed lines in the drawing) in the pixel regions[,] for displaying a desired picture when a voltage is applied to the scanning lines 10, to switch the TFT, and to transmit a picture signal provided to the signal lines 17 to the pixel electrodes.

Page 2, Paragraph beginning at line 13:

Referring to FIG. 1B showing a section across line A-A', the AMLCD is provided with a gate electrode 11 on a transparent substrate 7, and a gate insulating layer 13 on the gate electrode 11. There is a channel layer 15 and an ohmic contact layer 16 of amorphous silicon a-Si on the gate insulating layer 13, and source/drain electrodes 17a and 17b on the ohmic contact layer 16. There is a protection layer 19 on an entire surface of the source/drain electrodes 17a and 17b, a contact hole 20 in the protection layer 19. The pixel electrode 21 and the drain electrode 17b are connected through the contact hole 20. In the drawing, Cgs denotes a capacitance between the gate electrode and the source electrode, Cgd denotes a capacitance between the gate electrode and the drain electrode. The Ccross denotes a capacitance in overlap regions of the scanning lines and the signal lines. The Cgs, Cgd, and Ccross are parameters influencing to an accumulated capacitance (not shown), as well as Δ Vp (change in offset voltage) and Δ Vpxl (change in pixel voltage). In the related art LCD, if there is a [misalign] misalignment between the scanning line 10 and the signal line 17, minute variations of Cds and Cgd give influence to Δ

Vp and Δ Vpxl, making flicker worse and causing non-uniform luminance, that deteriorates a picture quality. And, in a divided exposure for a large sized screen, the increased deviations of Cgs and Cgd caused by poor adjustment between shots worsens the foregoing problem, to impede providing a large sized LCD screen, and, since the TFT is formed on an extension line of the scanning line, to reduce an aperture ratio of the device.

Page 3, Paragraph beginning at line 15:

[Other] Another object of the present invention is to provide TFT LCD which shows no deterioration of a picture quality even in divided exposure for a large sized screen.

Page 5, Paragraph beginning at line 12:

Referring to FIG. 2B, the LCD in accordance with a preferred embodiment of the present invention includes a scanning line (a gate electrode) 111 of a metal, such as aluminum, formed on a transparent substrate 107 by sputtering. There is an insulating layer 113 of SiNx or SiOx or the like formed thereon by APCVD (Atmospheric Chemical Vapor Deposition), and a semiconductor layer 115 and an n+ layer 115 stacked in succession thereon. The semiconductor layer 115 is formed of amorphous silicon a-Si, and the [n+ layer 116] insulating layer 113 is formed of SiO_2 having good bulk characteristics, and can prevent short circuit of the gate electrode 111 and formation of hillock at the gate electrode 11 without an anodized film. There are a channel layer and an ohmic contact layer [116] formed by etching the semiconductor layer 115 and the n+ layer 116, and source/drain electrodes 117a and 117b of aluminum or [chrome] chromium formed by sputtering and patterning. The ohmic contact layer 116 is formed by dry etching by using the source/drain electrode 117a and 117b as a mask. There is a protection layer 119 of SiNx on an entire surface of the substrate 107 formed by PECVD (Plasma Enhanced Chemical Vapor Deposition), and a pixel electrode 121 thereon in a pixel region formed by sputtering and patterning ITO (Indium Tin Oxide). The pixel electrode 121 is connected to the drain electrode 117b electrically through a contact hole 120 in the protection layer 119. The channel layer 115 has a width smaller than the [same] widths of the scanning line 111 and the signal line 117a, and is positioned between the scanning line 111 and the signal line 117a. In this instance, since the channel layer 115 is covered with the signal line 117a, generation of off-current is prevented, to prevent deterioration of a picture quality caused by a residual image. The

signal line 117a, serving as a source electrode of the TFT also, requires no extension pattern of the signal line as in the related art, and maintains a constant capacitance Ccross formed in an overlap region of the scanning line 111 and the signal line 117a. And, the signal line 117a maintains a constant capacitance Cgs between the scanning line 111 and the signal line 117a [constant] even if a misalignment [is occurred] occurs between the scanning line 111 and the signal line 117a. Since a pattern extended from the drain electrode 117b overlaps the scanning line 111 completely, even if there is a misalignment between the scanning line 111 and the signal line 117a, the capacitance between the scanning line 111 and the drain line 117b is always maintained constant [always]. Accordingly, the Δ Vp and Δ Vpxl involved in the effective voltage for driving the LCD are maintained constant owing to the Cgs, Cgd and Ccross, which are always constant regardless of the misalignment. In the drawing, 'δ' is greater than a movement caused by the misalignment of the scanning line 111 and the signal line 117a, 'Δ' is greater than a movement caused by the misalignment of the scanning line 111 and the channel layer 115, and ['α'] 'Δ' is greater than a movement caused by the misalignment of the signal line 117a and the channel layer 115.

In the claims

1. (Amended) A TFT LCD(thin film transistor liquid crystal display) comprising:

a first substrate and a second substrate;

a scanning line on the first substrate;

a signal line formed to cross the scanning line, wherein the signal line does not include an extension pattern;

a channel layer formed along the signal line and extended to a portion of the scanning line;

source and drain electrodes formed separated on the channel layer over the scanning line;

a pixel electrode connected to the drain electrode; and,

a liquid crystal layer formed between the first substrate and the second substrate.

2. (Amended) A TFT LCD(thin film transistor liquid crystal display) [as claimed in claim 1,] comprising:

a first substrate and a second substrate;

a scanning line on the first substrate;

a signal line formed to cross the scanning line;

a channel layer formed along the signal line and extended to a portion of the scanning line;

source and drain electrodes formed separated on the channel layer over the scanning line;

a pixel electrode connected to the drain electrode; and,

a liquid crystal layer formed between the first substrate and the second substrate;

wherein the drain electrode is parallel to the signal line.

8. (Amended) A TFT LCD comprising:

a first substrate and a second substrate;

a plurality of scanning lines on the first substrate;

a gate insulating layer on an entire surface inclusive of the scanning lines;

a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of [the] scanning lines;

source and drain electrodes formed separated on the channel layer over the scanning lines;

a signal line formed as a unit with the source electrode along the channel layer which is formed to cross the scanning lines, wherein the signal line does not include an extension pattern;

a protection film formed on an entire surface inclusive of the signal line;

a pixel electrode connected to the drain electrode on the protection film; and,

a liquid crystal layer formed between the first substrate and the second substrate.

15. (Amended) A TFT LCD having a first substrate, a second substrate, and liquid crystal sealed between the first and second substrates, comprising:

a scanning line on the first substrate;

a gate insulating layer on the scanning line;

a channel layer on the gate insulating layer;

a signal line formed to cross the scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern;

a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line;

a protection film formed on an entire surface of the first substrate inclusive of the drain electrode; and

a pixel electrode formed on the protection film connected to the drain electrode.

2. (Amended) A TFT LCD (thin film transistor liquid crystal display) [as claimed in claim 1,] comprising:

a first substrate and a second substrate;

a scanning line on the first substrate;

a signal line formed to cross the scanning line, wherein the signal line does not include an extension pattern;

a channel layer formed along the signal line and extended to a portion of the scanning line;

source and drain electrodes formed separated on the channel layer over the scanning line;

a pixel electrode connected to the drain electrode; and

a liquid crystal layer formed between the first substrate and the second substrate;

wherein the drain electrode is parallel to the signal line.

3. A TFT LCD as claimed in claim [1] 2, wherein the channel layer has a width smaller than a width of the signal line and the scanning line.

4. A TFT LCD as claimed in claim [1] 2, further comprising a gate insulating layer between the scanning line and the channel layer.

5. A TFT LCD as claimed in claim [1] 2, further comprising an ohmic contact layer between the source and drain electrodes and the channel layer.

6. A TFT LCD as claimed in claim [1] 2, wherein the source electrode and the signal line are formed as a unit.

7. A TFT LCD as claimed in claim [1] 2, wherein the drain electrode is overlapped with the scanning line.

9. (Amended) A TFT LCD [as claimed in claim 8,]comprising:

a first substrate and a second substrate;

a plurality of scanning lines on the first substrate;

a gate insulating layer on an entire surface inclusive of the scanning lines;

a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of scanning lines;

source and drain electrodes formed separated on the channel layer over the scanning lines;

a signal line formed as a unit with the source electrode along the channel layer which is formed to cross the scanning lines, wherein the signal line does not include an extension pattern;

a protection film formed on an entire surface inclusive of the signal line;

a pixel electrode connected to the drain electrode on the protection film; and,

a liquid crystal layer formed between the first substrate and the second substrate;

wherein the drain electrode is parallel to the signal line.

10. A TFT LCD as claimed in claim [8] 9, wherein the drain electrode crosses the scanning line.

11. A TFT LCD as claimed in claim [8] 9, wherein the channel layer has a width smaller than a width of the signal line and the scanning line.

12. A TFT LCD as claimed in claim [8] 9, further comprising an ohmic contact layer between the source and drain electrodes and the channel layer.

13. A TFT LCD as claimed in claim [8] 9, wherein the scanning line has a portion enlarged in the vicinity of the signal line.

15. (Amended) A TFT LCD having a first substrate, a second substrate, and liquid crystal sealed between the first and second substrates, comprising:

a scanning line on the first substrate;

a gate insulating layer on the scanning line;

a channel layer on the gate insulating layer;

a signal line formed to cross the scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern;

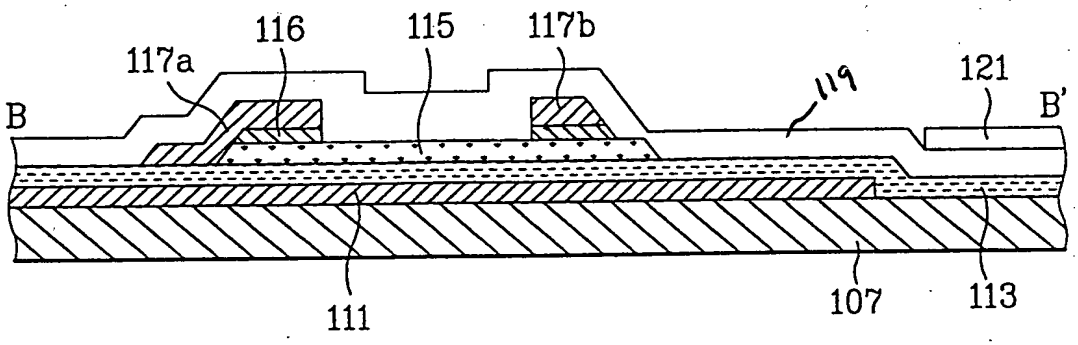
a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line;

a protection film formed on an entire surface of the first substrate inclusive of the drain electrode; and

a pixel electrode formed on the protection film connected to the drain electrode;

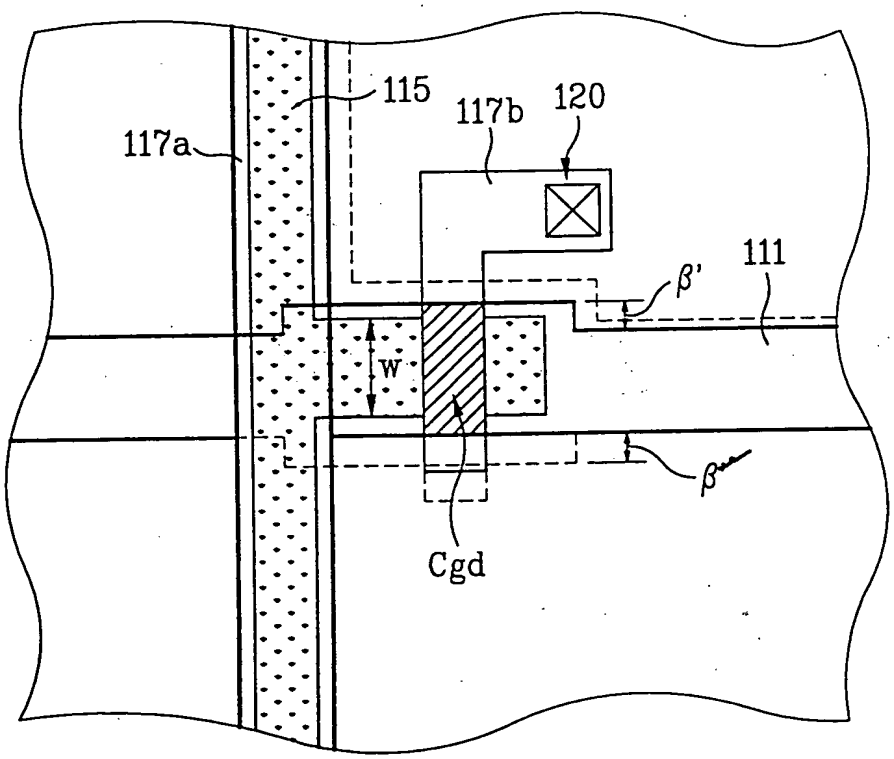
wherein the drain electrode is parallel to the signal line.

FIG. 2B



approved
Loke
8/6/02

FIG. 3



approved
Loke
8/6/02